Shobha Vasudevan

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Academic Appointments

Assistant Professor, University of Illinois at Urbana-Champaign, Electrical and Computer Engineering Department
Jan 2008 – present

Assistant Professor, University of Illinois at Urbana-Champaign, Computer Science Department
Jan 2011– present

Assistant Professor, University of Illinois at Urbana-Champaign, Information Trust Institute
Jan 2014– present

Visiting Professor, IIT Bombay, Mumbai
Summer 2010

Research Interests

Verification and security of hardware and embedded systems, Data mining techniques for reliability and security, Analog verification, Variation aware design and verification, Software testing, CAD for biomedical devices, Big data analytics- causality inferencing

Education

The University of Texas at Austin, PhD in Computer Engineering
Jan 2004 – Dec 2008
Graduate advisor: Dr. Jacob A. Abraham
PhD committee: E. Allen Emerson, Vijay Garg, Adnan Aziz, Jason Baumgartner

The University of Texas at Austin, M.S.E in Computer Engineering
Aug 2001 – Dec 2003

University of Mumbai, India, Bachelor of Engineering in Computer Engineering
Aug 1997 – Aug 2001

Achievements

IEEE Council of EDA Early Career Award, 2014
Dean's award for excellence in research in UIUC, 2014
Best paper award, VLSI Design 2014
ACM SIGDA outstanding new faculty award, 2013
Licensed a technology to Synopsys Inc. in 2012
NSF CAREER Award, 2010
Best paper award at forthcoming DAC 2014
GoldMine licensed by two leading EDA companies towards commercial product
YWCA leadership award in Science, 2011

Research Experience

Research Assistant w/ Dr. Jacob Abraham, CERC (Univ of Texas, Austin)
Jan 2002 – Dec 2008
Visiting Research Scholar at Intel Corporation, Intel Corp, Chandler, AZ
Jun 2004 – Sep 2004
Visiting Research Scholar at TIFR, School of Tech and CS, Mumbai, India

Jun 2005 – Aug 2005

Publications

Journal

- Shobha Vasudevan, E. A. Emerson and J. A. Abraham*. Improved Verification of Hardware Designs through Antecedent Conditioned Slicing*, International Journal on Software Tools and Technology Transfer (STTT), 9(1): 89-101 (2007). Invited paper, selected for journal special issue from AVOCS.
- Shobha Vasudevan, Vinod Viswanath, Robert Sumners and J. A. Abraham. *Automatic Verification of Arithmetic Circuits in RTL Using Stepwise Refinement of Term Rewriting Systems*, IEEE Transactions of Computers 56(10): 1401-1414 (2007)
- Shobha Vasudevan*,* Vinod Viswanath, J. A. Abraham, and Jiajin Tu. *Sequential Equivalence Checking of System Level and RTL Descriptions,* Design Automation for Embedded Systems (DAEM). 12(4): 377-396 (2008). Invited paper, selected for special journal issue from MEMOCODE.
- Vinod Viswanath, Shobha Vasudevan, Jacob A. Abraham*: Dedicated Rewriting: Automatic Verification of Low Power Transformations in Register Transfer Level*. Journal of Low Power Electronics 5(3): 339-353 (2009)
- Lingyi Liu, David Sheridan, William Tuohy and Shobha Vasudevan, *A Technique for Test Coverage Closure Using GoldMine*. IEEE Trans. on CAD of Integrated Circuits and Systems (IEEE TCAD)31(5): 790-803 (2012)
- Jayanand Asok Kumar and Shobha Vasudevan*. Formal performance analysis for faulty MIMO hardware.* IEEE Transactions on Very Large Scale Integrated Systems (IEEE TVLSI) 20(10): 1914-1918 (2012).
- Jayanand Asok Kumar and Shobha Vasudevan, SHARPE: *Variation-Conscious Formal Timing Analysis,* IEEE Transactions on CAD of Integrated Ciruits and Systems (IEEE TCAD), 32 (5): 788-801(2013)
- Samuel Hertz, David Sheridan and Shobha Vasudevan. *Mining Hardware Assertions With Guidance From Static Analysis* IEEE Trans. on CAD of Integrated Circuits and Systems 31 *(*IEEE TCAD*)* 32 (6): 952-965(2013)
- Lingyi Liu, and Shobha Vasudevan, *Automatic Generation of System Level Assertions from Transaction Level Models*. Accepted. Journal of Electronic Testing: Theory and Applications (JETTA) 29(5): 669-684 (2013)
- Jayanand Asok Kumar, Seyed Nematollah Ahmadyan and Shobha Vasudevan, *Efficient statistical model checking of hardware circuits with multiple failure regions.* Accepted. To appear in IEEE Transactions on CAD of Integrated Ciruits and Systems (IEEE TCAD)

Conference

- Shobha Vasudevan, E. A. Emerson and J. A. Abraham. *Efficient Model Checking of Hardware using Conditioned Slicing*, Automatic Verification of Critical Systems (AVOCS), 2004. Electr. Notes Theor. Comput. Sci. 128(6): 279-294 (2005)
- Shobha Vasudevan*,* Vinod Viswanath, J. A. Abraham, and Jiajin Tu*. Automatic Decomposition for Sequential Equivalence Checking of System*

Level and RTL Descriptions, International Conference on Formal Methods and Models for Codesign (MEMOCODE) 2006: 71-80

- Shobha Vasudevan*,* Vinod Viswanath, and J. A. Abraham . *Efficient Microprocessor Verification Using Antecedent Conditioned Slicing*, International Conference on (VLSI Design) 2007: 43-49
- Sankar Gurumurthy, Shobha Vasudevan and J. A. Abraham. *Automated Mapping of Pre-Computed Module-Level Test Sequences to Processor Instructions*, International Test Conference (ITC) 2005:10-20
- Sankar Gurumurthy, Shobha Vasudevan and J. A. Abraham. *Automated functional propagation of module level test responses,* International Test Conference (ITC) 2006: 1-9
- Shobha Vasudevan*,* Vinod Viswanath, J. A. Abraham, and Jiajin Tu . *Sequential Equivalence Checking of System Level and RTL Descriptions using Effective Compare Points*, Austin Conference of Integrated Systems and Circuits (ACISC) 2006.
- Vinod Viswanath, Shobha Vasudevan and J. A. Abraham. *Dedicated Rewriting: Automatic Verification of Low Power Transformations in RTL,* International Conference on VLSI Design *(*VLSI Design) 2009: 77-82
- Shobha Vasudevan, David Sheridan, Sanjay Patel, Bill Tuohy. *GoldMine: Automatic generation of assertions using data mining and static analysis*, Design Automation and Test in Europe (DATE) 2010:626-629
- Lingyi Liu and Shobha Vasudevan *STAR: Generating Validation Inputs by Static Analysis of RTL*, International High Level Design Validation and Test Workshop (HLDVT) 2009: 32-37
- Jayanand Asok Kumar and Shobha Vasudevan *Automatic compositional reasoning for probabilistic model checking of hardware designs*, International Conference on Quantitative Evaluation of Systems (QEST) 2010:
- Viraj Athavale, Jayanand Asok Kumar and Shobha Vasudevan *A Scalable Approach for Throughput Estimation of Timing Speculation Designs,* MWSCAS 2010
- Jayanand Asok Kumar and Shobha Vasudevan *Statistical Guarantees of Performance for MIMO Designs*, International Conference on Dependable Systems and Networks (DSN) 2010:
- Shobha Vasudevan: Coverage closure in SoC verification: Are we chasing a mirage? VLSI Test Symposium (VTS)2011
- Jayanand Asok Kumar and Shobha Vasudevan, *Variation-Conscious Formal Timing Verification in RTL,* International Conference o*n* VLSI Desig*n (*VLSI Design) 2011:58-63
- Lingyi Liu, David Sheridan, William Tuohy, Shobha Vasudevan *Towards coverage closure: Using GoldMine assertions for generating design validation stimulus*, Design Automation and Test in Europe (DATE) 2011: 173-178
- Lingyi Liu and Shobha Vasudevan *Efficient validation input generation in RTL using hybridized source code analysis*, Design Automation and Test in Europe (DATE) 2011: 1596-1601
- Lingyi Liu, David Sheridan, Viraj Athavale, Shobha Vasudevan: *Automatic generation of assertions from system level design using data mining*, , International Conference on Formal Methods and Models for Codesign (MEMOCODE) 2011: 191-200
- Jayanand Asok Kumar Lingyi Liu and Shobha Vasudevan, *Scaling Probabilistic Timing Verification of Hardware Using Abstractions in Design*

Source Code, Formal Methods in Computer Aided Design, (FMCAD) 2011: 196-205

- Shobha Vasudevan, *GoldMine: Automatic assertion generation using data mining and static analysis,* Design and Verification Conference*, (*DVCON) 2011
- Parth Sagdeo, Viraj Athavale Sumant Kowshik and Shobha Vasudevan *PRECIS: Inferring Invariants using Program Path Guided Clustering,* International Conference on Automated Software Engineering (ASE) 2011: 532-535
- Hyungsul Kim, David Sheridan, Sungjin Im, Shobha Vasudevan, Tarek Abdelzaher and Jiawei Han*, Signature Pattern Covering via Local Greedy Algorithm and Pattern Shrink,* , 2011 International Conference on Data Mining (ICDM) 2011: 330-339
- Jayanand Asok Kumar and Shobha Vasudevan: *Verifying dynamic power management schemes using statistical model checking*. Asia South Pacific Design Automation Conference (ASP-DAC) 2012: 579-584
- Jayanand Asok Kumar, Kenneth M Butler, Heesoo Kim and Shobha Vasudevan, *Early prediction of NBTI effects using RTL source code analysis,* Design Automation Conference *(*DAC) 2012: 808-813
- Seyed Nematollah Ahmadyan, Jayanand Asok Kumar and Shobha Vasudevan, *Goal-oriented stimulus generation for analog circuits,* Design Automation Conference *(*DAC) 2012: 1018-1023
- Viraj Athavale,Sam Hertz, Darshan Jetly, Vijay Ganesan, Jim Krysl and Shobha Vasudevan, *Using static analysis for coverage extraction from emulation/prototyping platforms,* IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis*, (*CODES+ISSS) 2012: 207-214
- Lingyi Liu, Chen Hsuan Lin and Shobha Vasudevan*, Word Level Feature Discovery to Enhance Quality of Assertion Mining,* International Conference on Computer Aided Design *(* ICCAD) 2012: 210-217
- Seyed Nematollah Ahmadyan and Shobha Vasudevan, *Reachability Analysis of Nonlinear Analysis through Iterative Reachable Set Reduction*, Design Automation and Test in Europe (DATE) 2013: 1436-1441
- Seyed Nematollah Ahmadyan and Shobha Vasudevan, *Runtime Verification of Nonlinear Analog Circuits Using Incremental Time-Augmented RRT Algorithm*, Design Automation and Test in Europe (DATE) 2013: 21-26
- Chen-Hsuan Lin, Lingyi Liu and Shobha Vasudevan, *Generating concise assertions with complete coverage*, ACM Great Lakes Symposium on VLSI (GLSVLSI) 2013, pp 185-190
- Lingyi Liu, Shobha Vasudevan, *Scaling RTL property checking using feasible path analysisand decomposition*, ACM Great Lakes Symposium on VLSI (GLSVLSI) 2013, pp 173-178
- Parth Sagdeo, Nicholas Ewalt, Debjit Pal and Shobha Vasudevan, *Using Automatically Generated Invariants for Regression Testing and Bug Localization*, International Conference on Automated Software Engineering (ASE) 2013: 634-639
- Seyed Nematollah Ahmadyan and Shobha Vasudevan, *Efficient Stochastic SAT Solving Using Random Graphs*. Invited paper in Workshop for Constraints in Formal Verification (CFV), 2013
- Lingyi Liu, Xuanyu Zhong, Xiaotao Chen and Shobha Vasudevan, *Diagnosing Root Causes of System Level Performance Violations,*

International Conference on Computer Aided Design *(*ICCAD) 2013: 295-302

- David Sheridan, Lingyi Liu, Hyungsul Kim and Shobha Vasudevan , *A Coverage Guided Mining Approach for Automatic Generation of Succinct Assertions*. In Proceedings of International Conference on VLSI Design (VLSI Design) 2014 . Best paper award.
- Viraj Athavale, Sai Ma, Samuel Hertz and Shobha Vasudevan, *Code Coverage of Assertions Using RTL Source Code Analysis*. To appear in Design Automation Conference (DAC) 2014. Best paper award.

Book chapter/Theses

- Shobha Vasudevan and Jacob A. Abraham*. Static Program Transformations for Efficient Software Model Checking,* Book chapter in World Congress of Computers (WCC), 2004. IFIP Congress Topical Sessions 2004: 257-282
- Shobha Vasudevan*. Automatic Verification of Arithmetic Circuits in RTL Using Term Rewriting Systems*, Masters Thesis, December 2003, The University of Texas at Austin.
- Shobha Vasudevan. *Static analysis of high level descriptions in hardware for taming verification complexity*, PhD Thesis, May 2008, The University of Texas at Austin.

Industrial Impact

- Patent (pending) Title: INTEGRATION OF DATA MINING AND STATIC ANALYSIS FOR HARDWARE DESIGN VERIFICATION. U.S. Patent Application No. 20130019216
- Patent (pending): Title: MERIT BASED CHARACTERIZATION OF ASSERTIONS. U.S Patent Application No. 14/031,949
- Evaluation license agreements for GoldMine with 2 EDA and 3 semiconductor companies
- Licensing of GoldMine to a leading EDA company towards commercial product development
- Collaborators: Ken Butler, John Carulli (Texas Instruments, Dallas), Alan Gatherer (Huawei Technologies, Dallas), Raghuram Tupuri (AMD), Eli Chiprout , Chengie Gu and Suriya Natarajan (Intel, Portland), Manish Gajjar (Broadcom, San Jose), Jim Krysl (Qualcomm Inc., San Diego)
- Invited to DVCon 2011 as a speaker. GoldMine selected as one of most popular tools

Outreach Activities

- Founder of MyTri, a professional networking portal for mentoring women engineers in Illinois: a Facebook and Linkedin application. Initiative funded by ECE department at Illinois. Portal development and pilot deployment in Women in ECE and Women in CS groups at UIUC
- Invited to CRAW/CDC Wokshop on Diversity in Design Automation co-located with DAC 2014 as a plenary speaker
- Nominated and elected as Vice Chair for Women in Electronic Design for DAC 2012. This group conducts the workshop for women in EDA at the Design Automation Conference every year
- Active mentoring of female undergraduate students for applying to graduate school. Won YWCA award for leadership in Science for mentoring efforts
- Organizer of the SIGDA-NSF-ACM Design Automation Summer School collocated with DAC 2011
- Organizer of the TTTC's Ed McCluskey Best Doctoral Thesis award for PhD

students in VLSI Test Symposium
- Organizer of a panel in VLSI Test Symposium “Coverage Closure in SoC Verification: Are we Chasing a Mirage?”

Invited Talks

- ACM CRAW (Computer Research Association's Committee on Women) and CDC (Coalition to Diversify Computing) Workshop on Design Automation: Plenary speaker
- *Automatic Assertion Generation: Experience, Value and Some Wisdom*, Rice University, Nov 2013
- *Automatic Assertion Generation: Experience, Value and Some Wisdom*, Princeton University, Oct 2013
- *Automatic Assertion Generation: Experience, Value and Some Wisdom*, Penn State University, Oct 2013
- *Automatic Assertion Generation: Experience, Value and Some Wisdom*, Carnegie Melon University, May 2013
- *Automatic Assertion Generation: Experience, Value and Some Wisdom*, Stanford University, May 2013
- *Automatic Assertion Generation: Experience, Value and Some Wisdom*, University of California at Berkeley, May 2013
- *Verification and Validation at Illinois*, Invited lecture at Synopsys Inc., Mountain View, CA, November 2011
- *GoldMine: Automatic Assertion Generation and Achieving Test Coverage Closure*, Distinguished CECS seminar at University of California at San Deigo, UCSD, June 2011
- *GoldMine: Automatic Assertion Generation and Achieving Test Coverage Closure,* Invited talk at University of California at Irvine, June 2011
- *GoldMine: Automatic Assertion Generation and Achieving Test Coverage Closure*, Univ of California at Santa Barbara, May 2011
- *GoldMine: Automatic Assertion Generation and Achieving Test Coverage Closure*, Distinguished seminar at TIMA, Grenoble, March 2011
- *GoldMine: Automatic Assertion Generation and Achieving Test Coverage Closure,* Invited talk at Virginia Tech, March 2011
- *GoldMine assertions for post-Si validation*, Invited special session talk at ITC 2010, Austin, TX
- *Toward Coverage Closure Using GoldMine*, Invited talk at Huawei Technologies, Dallas, April 2010
- *STAR: Generating Validation Inputs by Static Analysis of RTL,* Invited talk at High Level Design, Validation and Test workshop, Nov 2009, San Francisco, California.
- *Early bird finds the bug: Verification using static analysis at RT-level*, Invited talk at Advanced Micro Devices (AMD), Austin, October 2009
- *Early bird finds the bug: Verification using static analysis at RT-level*, Invited talk at Qualcomm Inc., San Diego, November 2009
- *GoldMine: Automatic Assertion Generation*, Invited talk at Texas Instruments (TI), Dallas, October 2009

Teaching

Logic Design (Undergraduate) (Spring 2008, Spring 2009, Fall 2010, Fall 2011, Fall 2012, Fall 2013)
Formal Hardware and SoC Verification (Graduate) (Fall 2008, 2009)
Introduction to Computer Engineering (Undergraduate) (Spring 2010, Spring 2011,

Spring 2013)

Students

PhD students: Jayanand Asok Kumar (Qualcomm Inc.), Lingyi Liu (Synopsys Inc.), Adel Ahmadyan, Debjit Pal
Masters: David Sheridan (NVIDIA), Viraj Athavale (Oracle), Parth Sagdeo, Samuel Hertz (Apple Inc.), Sai Ma
Undergraduate: Doupamo Eradiri, Rohit Mehta, Tong Qi, Nick Ewalt, Aniruddh Rangarajan, Hee Soo Kim, Xuanyu Lin, Tian Xia, Miguel De Dios, Sai Kaladidndi, Yangdong Li, Sai Koppula, Itir Akgun, Paul Logsdon, Hyun Yi
PhD committee: Vladimeros Vladimerou, Long Wang, Gabriela Jacques De Silva, Matthew Hicks, Qiang Ma

Research Grants

NSF CAREER 2010–2014
NSF Cyberphysical systems (Collaborative) 2010–2013
Qualcomm Inc. 2010–2011
Huawei Technologies 2011–2014
Boeing Corporation 2012–2015
NSA lablet for security 2011–2013
Synopsys Inc. 2011–2013
Intel Corporation 2014
NSF CCF SHF: Small 2014-2017

Program Committees

DAC 2014, ITC 2014, DAC 2013, MEMOCODE 2012, DATE 2012, VLSI Conference 2012, ICCD 2011, ISCA 2011, General Chair of IWLS 2013, HVC 2014, DAC 2014

Industrial Experience

Internship, Functional Verification and Testing, Motorola, Austin
Jun 2002 – Sep 2002
Internship, Formal Verification Group, Intel Corp, Austin
May 2003 – Aug 2003
Internship, Functional Testing Group, Intel Corp, Chandler
June 2004 – Sep 2004
Internship, Verification Research Division, Qualcomm Inc, Austin
Feb 2006 – May 2006

Refereed Forums

IEEE Transactions on Computers
International Journal on Software Tools and Technology Transfer
IEEE VLSI Test Symposium
Design, Automation and Test in Europe
International Test Conference
International Conference on Computer Aided Verification
International Conference on Computer Aided Design

Professional Societies

Senior Member of the IEEE

Member of the ACM